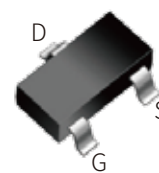


FEATURES

- | $V_{DS} = -30V, I_D = -4.1A$
- | $R_{DS(ON)} < 46\text{ m}\Omega @ V_{GS} = -10V$
- | $R_{DS(ON)} < 72\text{ m}\Omega @ V_{GS} = -4.5V$
- | Trench Power LV MOSFET technology
- | High density cell design for low $R_{DS(ON)}$
- | High Speed switching
- | Meet AEC-Q101 Requirements



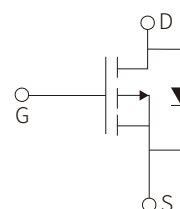
SOT-23



Marking

APPLICATION

- | Battery protection
- | Load switch
- | Power management



Schematic Symbol

APPROVALS

RoHS	Compliance with 2011/65/EU
HF	Compliance with IEC61249-2-21:2003

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate Threshold Voltage	V_{GSS}	± 20	V
Drain Current - Continuous ($T_A = 25^\circ\text{C}$)	I_D	-4.1	A
Drain Current - Continuous ($T_A = 70^\circ\text{C}$)		-3.2	
Pulsed Drain Current ^A	I_{DM}	-15	A
Power Dissipation ($T_A = 25^\circ\text{C}$)	P_D	1.2	W
Power Dissipation ($T_A = 70^\circ\text{C}$)		0.8	
Thermal Resistance Junction- to- Ambient ^B	$R_{\theta JA}$	105	$^\circ\text{C/W}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (Ta=25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate-source leakage current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$			-1	μA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-1.5	-2.0	V
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-3A$		41	46	m Ω
		$V_{GS}=-4.5V, I_D=-2A$		64	72	m Ω
Diode Forward Voltage	V_{SD}	$I_S=-4.1A, V_{GS}=0V$			-1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$		572		pF
Output Capacitance	C_{oss}			82		pF
Reverse Transfer Capacitance	C_{rss}			70		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DS}=-15V$ $V_{GS}=-10V, R_{GEN}=2.5\Omega$ $R_L=15\Omega$		3.8		ns
Turn-on Rise Time	t_r			17.6		ns
Turn-Off Delay Time	$t_{d(off)}$			17.8		ns
Turn-off Fall Time	t_f			21.8		ns
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-4.1A$ $V_{GS}=-10V$		11.65		nC
Gate-Source Charge	Q_{gs}			2.32		nC
Gate-Drain Charge	Q_{gd}			2.08		nC
Reverse Recovery Chrage	Q_{rr}	$I_F=-10A, di/dt=100A/us$		0.643		nC
Reverse Recovery Time	t_{rr}			15.7		ns

A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

PARAMETER CHARACTERISTIC CURVE

Fig 1: Output Characteristics

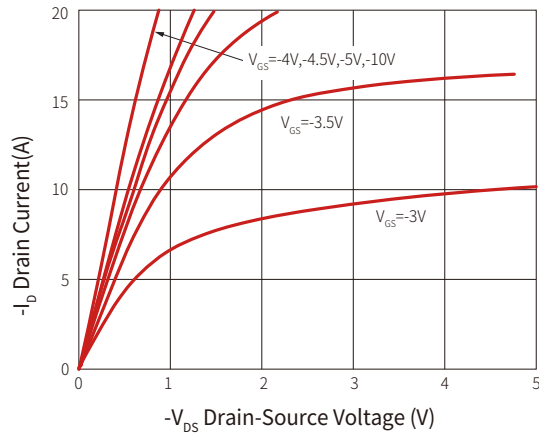


Figure 2: Transfer Characteristics

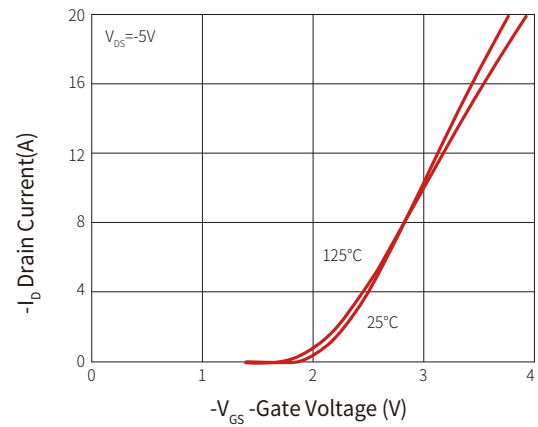


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

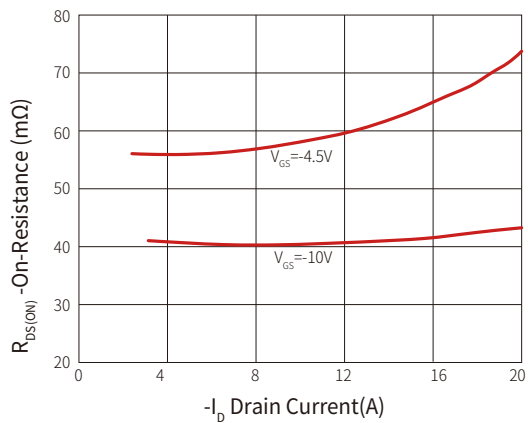


Figure 4: On-Resistance vs. Junction Temperature

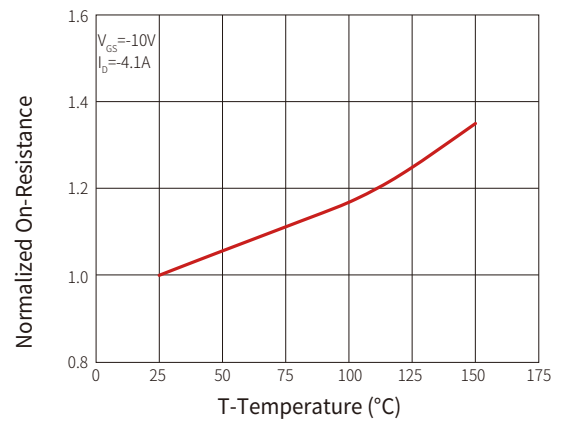


Figure 5: Capacitance Characteristics

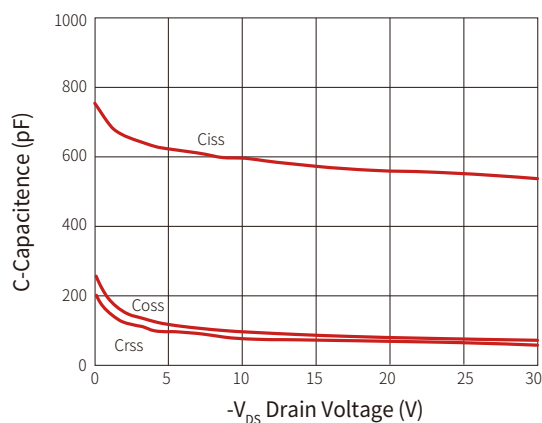


Figure 6: Gate Charge

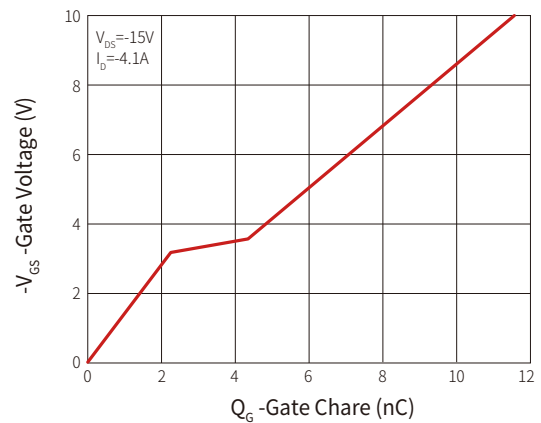


Figure 7: Safe Operation Area

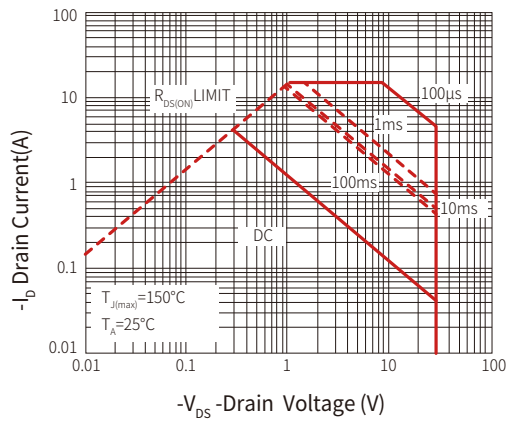


Figure 8: Maximum Continuous Drain Current vs Ambient Temperature

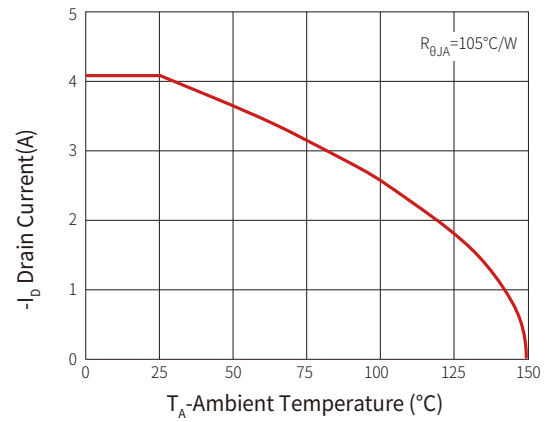
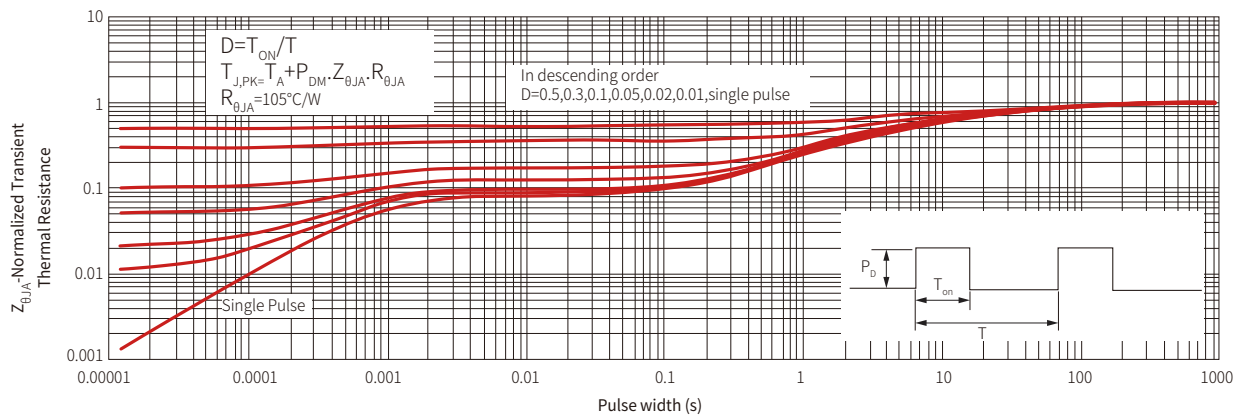
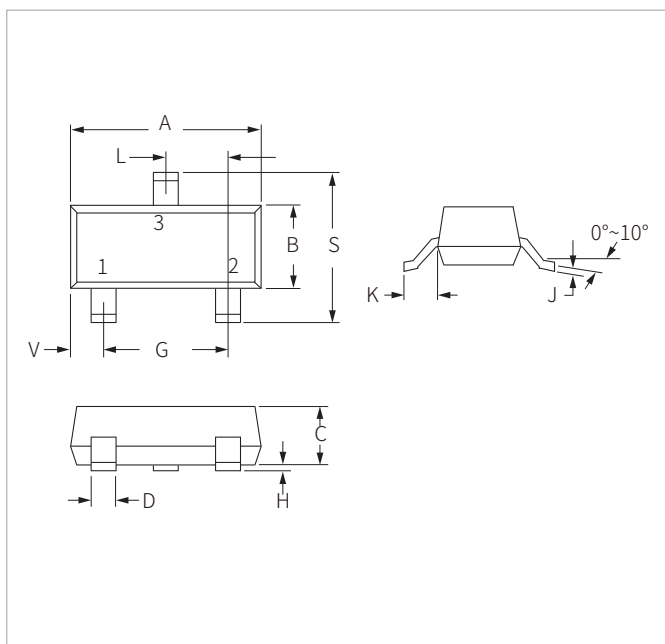


Figure 9: Normalized Maximum Transient Thermal Impedance

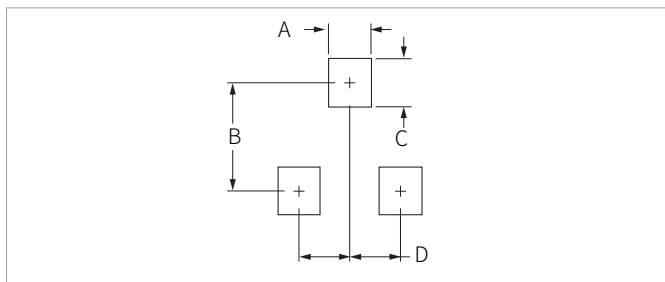


SOT-23 PACKAGE INFORMATION



Ref.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.80	3.05	0.110	0.120
B	1.20	1.60	0.047	0.063
C	0.90	1.15	0.035	0.045
D	0.37	0.50	0.015	0.020
G	1.75	2.05	0.069	0.081
H	0.01	0.100	0.001	0.004
J	0.085	0.180	0.003	0.007
K	0.35	0.69	0.014	0.029
L	0.89	1.02	0.035	0.040
S	2.10	2.65	0.083	0.104
V	0.45	0.60	0.018	0.024

RECOMMENDED PAD LAYOUT DIMENSIONS



Ref.	Millimeters		Inches	
	Min	Max	Min	Max
A	0.71	0.97	0.028	0.038
B	1.88	2.13	0.074	0.084
C	0.71	0.97	0.028	0.038
D	0.81	1.07	0.032	0.042

ORDERING INFORMATION

Part Number	Component Package	QTY/Reel	Reel Size
SPM3407SQ	SOT-23	3000PCS	7"

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By QR Code

Website



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